UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,641	05/09/2006	Adrianus Marinus Gerardus Peeters	NL 031311	1751

24737 7590 05/16/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

MAIL DATE	DELIVERY MODE
05/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Tran

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Office Action Summary	Application No.	Applicant(s)	
	10/578,641	PEETERS ET AL.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,8,10 and 11* is/are rejected.

7)☒ Claim(s) *4-6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 5/9/2006

2. Claims 1-11 are pending for examination.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. "adding respective delays to a source clock signal".

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. "the clock generator is low enough in order to ensure"

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Smith et al. US 20030079150 ("Smith").

11. As per claim 1, Smith discloses an electronic circuit [fig. 7] according to claim 8, further comprising:

a plurality of storage elements [transition-once buffer 710-716] arranged for storing of data elements,

a plurality of processing element [logic units 702-708] arranged for processing data elements stored in the plurality of storage elements,

wherein storage elements of the plurality of storage elements are further arranged to load their data elements at respective points in time of a first set of point in time [fig. 8], and wherein the points in time are mutually different in order to meet a maximum allowable value of the

power consumption peaks [claim 13 – *delay execution unit to meet a maximum allowable value of the power consumption peaks*].

12. As per claim 10, Smith discloses a method of processing data elements, the method comprising:

determining a first set of points in time, in a first operating mode, for storing data elements in respective storage elements [transition-once buffers 710-716] of a plurality of storage elements [claim 13],

generating output data elements each by performing respective logic operation [702-708] on respective data elements,

wherein the points in time of the first set of points in time at which respective storage elements load their data elements are mutually different in order to meet a maximum allowable value of the power consumption peaks [fig. 8].

13. Claims 1, 10 rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. US. 2004/0068684 ("Huang")

14. As per claim 1, Huang discloses an electronic circuit [fig. 1] according to claim 8, further comprising:

a plurality of storage elements [110a-110c fig. 1] arranged for storing of data elements,

a plurality of processing element [126a-126c] arranged for processing data elements stored in the plurality of storage elements,

wherein storage elements of the plurality of storage elements are further arranged to load their data elements at respective points in time of a first set of point in time [130a-130b fig. 1], and wherein the points in time are mutually different in order to meet a maximum allowable value of the power consumption peaks [paragraph 0008-0010; fig. 2].

15. As per claim 2, Huang discloses the electronic circuit further comprises:

a clock generator [TCLK fig. 1] arranged to generate period clock signal,

delay elements [130a-130b fig. 1] arranged to generate a point in time of the first set for a respective one of the storage elements by adding respective delays to a source clock signal, wherein the respective delays are mutually different [*RAM 110b delayed by delay unit 130a, RAM 110c delayed by delay unit 130a+130b*].

Endo does not explicitly teach the frequency of the clock generator is low enough in order to ensure data integrity during processing of the data elements. However, this feature is deemed to be inherent to the Endo's clock generator since the system of Endo would be inoperable if the frequency of the clock generator is not properly calibrated.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

18. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claims 3, 7-8, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith as applied to claim 1 above, and further in view of Durham et al. U.S. Patent No. 5,737,614 ("Durham").

20. As per claim 3, Although Smith teaches a method for reducing power consumption in an electronic circuit by delaying the activating of a logic circuit so that the total power will not exceeds the power budget. However, Smith does not explicitly teach a timing circuit arranged to determine the set of delay time for different operating mode.

Durham teaches another invention relates to the dynamic regulation of power consumption in self-timed circuits. More particularly, the present invention regulates the frequency in order to control power consumption in a self-timed circuits having plural pipeline stages. Specifically, Durham teaches a timing circuit arranged to determine the first set of points in time [35, 45 fig. 3B]in a first operating mode [*slow mode to relieve excessive power conditions – col. 5 lines 28-34*], in a second operating mode [fast mode – col. 5 lines 33-53-67], at which respective storage elements [10-40 fig. 3A-B] load their data elements, wherein the

respective points in time of the second set of points in time are essentially identical [line 17, 27, 37, 47 NO delay], and

wherein the timing circuit is further arrange to select an operating mode depending on control signal [lp_in fig. 3A].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Smith with the arrangement to determine the first set of points in time for a first operating mode and a second set of points in time for a second operating mode depending on a control signal as taught by Durham. The motivation for doing so would have been to provide the system the ability to dynamically maximize the operating speed of the system in responding to the maximum allowable value of the available power.

21. As per claim 7, Durham further teaches

handshake channel [11, 21, 31, 41 fig. 1A-B] arranged for communication between storage elements of the plurality of storage elements and processing elements of the plurality of processing elements,

delay elements arranged to generate a point in time of the first set for a respective one of the storage elements by adding respective delays to a request signal for loading of the data elements, wherein the delays are mutually different [18, 28 fig. 3A].

22. As per claim 8, Durham further teaches

handshake channels [11, 21, 31, 41 fig. 1A-B] arranged for communication between storage elements of the plurality of storage elements and processing elements of the plurality of processing elements,

a first handshake component [22 fig. 1A] arranged to receive a request signal, in a first operating mode, for loading of data elements and in response thereto to generate a request signal for respective one of the storage elements of the plurality of storage elements for loading of data elements at respective points in time of the first set of points in time [see fig. 3A-B].

Allowable Subject Matter

23. Claims 4-6, 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Examiner's note:

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.